IN THE CLAIMS

Please amend the claims as follows:

Claims 1-22 (Canceled).

Claim 23 (Currently Amended): A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order, the semiconductor substrate being in contact with the insulating layer;

an isolation insulating film formed in a main surface of said semiconductor layer;

a first semiconductor element formed in an element formation region defined by said isolation insulating film in said semiconductor layer, said first semiconductor element including source/drain regions formed in contact with said insulating layer;

an interlayer insulating film formed on said first semiconductor element and said isolation insulating film;

~~at least one of a power supply line and a ground line formed on said interlayer insulating film;~~

~~a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line;~~

a second semiconductor element formed adjacently to said first semiconductor element in said semiconductor layer, having an operating threshold voltage different from that of said first semiconductor element; and

a ~~second~~ complete-isolation insulation film formed extending from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer between said first semiconductor element and said second semiconductor element.

Claim 24 (Previously Presented): A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order, the semiconductor substrate being in contact with the insulating layer;

an isolation insulating film formed in a main surface of said semiconductor layer;

a first semiconductor element formed in an element formation region defined by said isolation insulating film in said semiconductor layer, said first semiconductor element including source/drain regions formed in contact with said insulating layer;

an interlayer insulating film formed on said first semiconductor element and said isolation insulating film;

~~at least one of a power supply line and a ground line formed on said interlayer insulating film;~~

~~a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line;~~

a second semiconductor element formed adjacently to said first semiconductor element in said semiconductor layer, having an operating frequency different from that of said first semiconductor element; and

a ~~second~~ complete-isolation insulating film formed extending from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer between said first semiconductor element and said second semiconductor element.

Claim 25 (Previously Presented): A semiconductor device comprising:

an SOI substrate having a structure in which a semiconductor substrate, an insulating layer and a semiconductor layer are layered in this order, the semiconductor substrate being in contact with the insulating layer;

an isolation insulating film formed in a main surface of said semiconductor layer;

a first semiconductor element formed in an element formation region defined by said isolation insulating film in said semiconductor layer, said first semiconductor element including source/drain regions formed in contact with said insulating layer;

an interlayer insulating film formed on said first semiconductor element and said isolation insulating film;

~~at least one of a power supply line and a ground line formed on said interlayer insulating film;~~

~~a first complete-isolation insulating film formed throughout a portion directly below at least one of said power supply line and ground line;~~

a bonding pad formed on said interlayer insulating film for electrically connecting said first semiconductor element and an outer element; and

a ~~second~~ complete-isolation insulating film formed extended from said main surface of said semiconductor layer, reaching said upper surface of said insulating layer below said bonding pad.